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Power integrity analysis challenges on Networking devices

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The power integrity analysis for Networking Processor Chips is facing multiple challenges. This presentation will address the most critical ones which are the design complexity increase and voltage noise reduction.

A real device example with 96 SERDES lanes at 56Gbps PAM4, with multiple sub 1V supplies and > 200W total power, will be used to show how to cope with its power integrity analysis, considering the availability of models, their accuracy, the runtime and the result exploration capability.

An outlook of challenges to be solved by the scientific and EDA community, to enable the next generation networking processor developments, will close the presentation.