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Signal and Power Integrity Design Challenges In High End Servers

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The presentation will show the signal and power integrity challenges of the latest IBM z15 server announced in September 2019. This includes technical details about system architecture, data bandwidths and signal speeds as well as the power integrity design of the processor board. On SI the technology attributes will be given to achieve the high bandwidths and density on the first and second level packaging. For power integrity a measurement example will be shown, where the power noise is generated just by starting multiple cores simultaneously.